NEGATIVE RESISTANCE OPTIMIZED IN NOISE FOR LOSSES COMPENSATION IN MICROSTRIP RESONATORS

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ABSTRACT

A new design concept of low noise negative resistance circuit is presented considering stability conditions. Low noise properties of a negative resistance circuit are guarantied by an optimal value of the transistor feedback. Based on this circuit, a low-noise 2^{nd}-order 3GHz active bandpass filter has been designed and fabricated.

I. INTRODUCTION

With the rapid expansion of new applications, such as mobile communications, microwave engineers have found great advantage in using active filters. Nevertheless, the use of active elements in microwave filters has introduced new design parameters and problems such as electrical stability, power handling behavior and noise figure. Microwave active filters (MAF) using negative resistance circuits (NRC) to compensate for the losses of passive resonators have been described by many researchers. However, few authors analyze the noise behavior of such filters [1–4]. Reported noise figure values are high. One example of noise reduction in MAF using NRCs has been considered in [5]. The problem solution was achieved by choosing the best location of given NRCs within the resonators. In the paper presented here, the noise reduction in the MAF structure using a NRC is reached with the reduction of the noise of the NRC itself through the optimization of the transistor feedback. A preliminary study on the subject is presented in [6], but with no extension to the noise minimization problem for MAF applications. In this paper, we present a simulator-oriented approach for the design of low noise NRCs. An experimental validation using this NRC is presented with the design of a 2nd order narrow band MAF.

II. THEORY

The conceptual factor that describes the noise properties of the NRC is the noise measure M. Definition of M (for N-port devices) was done in [7, pp.78, formula 4.109] and can be rewritten for NRC (single port case) as follows:

$$M = -\frac{C}{k \cdot T \cdot (1-|S|^2)} \tag{1}$$

where C is the spectral density of the noise power excited by NRC, S is the complex reflection coefficient of the NRC, T is the absolute temperature (in Kelvin) and k is the Boltzmann constant.

Basic principle of losses compensation with a negative resistance is presented in Fig.1.

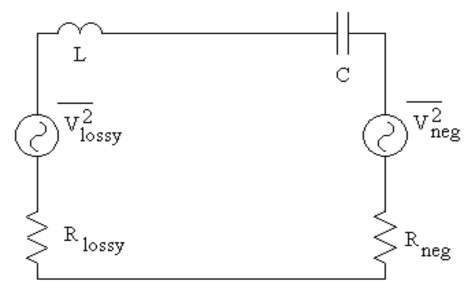

Fig.1. Compensation for losses in a resonator

Negative resistance value equals the resistance value associated with the losses in a resonator. The total noise voltage source spectral density V^2 in the resonator can be found as the sum of the two spectral densities (depicted in Fig.1) of the noise voltage source associated with the lossy resistor and the noise voltage source associated with the negative resistor:

$$\overline{V^2} = \overline{V^2_{lossy}} + \overline{V^2_{neg}} \tag{2}$$

The first term in the sum can be found using a noise wave technique [7, pp.55] and Bosma's theorem [8]. The second term in the sum can be found using formula (1) and the same noise wave technique.

Then, relation (2) gives:

$$\overline{V^2} = 4 \cdot k \cdot T \cdot R_{lossy} + 4 \cdot k \cdot T \cdot |R_{neg}| \cdot M \tag{3}$$

If $R_{neg} + R_{lossy} = 0$, the expression (3) becomes:

$$\overline{V^2} = 4 \cdot k \cdot T \cdot R_{lossy} \cdot (1+M) \tag{4}$$

It can be noted in formula (4) that, if M >>1, the noise in the resonator is the noise of active device. If M<<1, the noise in the resonator is the noise due to passive parts only. So, in the case where losses of a passive filter are compensated using NRCs, minimization of the M value determine the noise performances of the corresponding MAF structures. Basic schematic of the FET-based NRC is depicted in Fig.2.

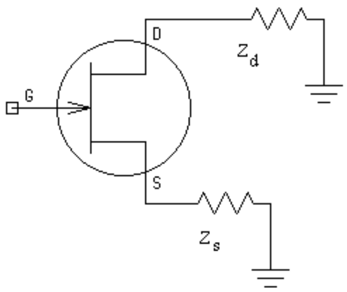

Fig.2. NRC basic configuration

The negative resistance effect is achieved at the gate of a single FET loaded by impedances Zd and Zs on the drain and on the source respectively. In our study, we assume that:

a) Zd and Zs are complex impedances.

b) Zd and Zs values should be chosen properly to satisfy the condition for the stability of the NRC over the total FET operating frequency band.

c) Zd and Zs values should be chosen to be able to obtain a minimum value of *M* over the NRC operating frequency band to achieve low noise performances.

It is shown in [6] that, if Zd and Zs are lossless, the values of Zd and Zs can be determined in an exact analytical form to reach the minimum value of M. But, this analytical solution for Zd and Zs is not applicable in our case due to the ideal nature of Zd and Zs and cannot be used to estimate the noise measure of the active device itself. So our approach consists of a novel formulation of the optimization problem that can be used with classical CAD package to find the impedance values of Zd and Zs.

Basically, circuit simulators do not allow modeling and optimization of the *M* value. So, the auxiliary schematic in Fig.3 is proposed to optimize NRC with minimum *M* goal. The noise figure value *Nf* of the circuit in Fig.3 can be obtained with formula (1) and the noise wave technique of [7, pp.55]:

$$Nf = 1 - M \cdot \frac{\mathrm{Re}(Z_{11})}{R_g} \tag{5}$$

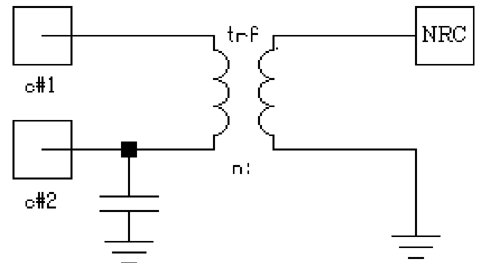

Fig.3. Auxiliary schematic for NRC noise measure minimization

where Z_{11} is the corresponding input parameter of the NRC circuit and Rg is the port c#1 impedance value (Fig.3).

Then the M value of the NRC can be written into the following form:

$$M = \frac{R_g}{\mathrm{Re}(Z_{11})} - Nf \cdot \frac{R_g}{\mathrm{Re}(Z_{11})} \tag{6}$$

Note in (6) that, because $\mathrm{Re}(Z_{11})$ of the NRC is negative, the minimum value of *M* is obtained for a minimum value of *Nf*, when R*g* and $\mathrm{Re}(Z_{11})$ are considered constant. Then, the optimization goal can be formulated as follows:

$$Nf \to 0 \;\; and \;\; \mathrm{Re}(Z_{11}) \to \ldots some\ negative\ value \tag{7}$$

Because any changes in impedance values Zd and Zs during the optimization procedure can cause changes for both Z_{11} and *Nf* values, the transformer coefficient (Fig.3) is optimized to maintain the negative constant value of $\mathrm{Re}(Z_{11})$.

III. LOW NOISE NRC DESIGN EXAMPLE

To validate our concepts, a planar NRC has been designed on a Duroid substrate (ε =2.32, h=790um, copper thickness t=9um). The S-parameters linear model of the FHX35LG low noise FET and the nonlinear model of the same FET available from Ansoft [9] were used to design the NRC at 3GHz. The NRC topology used for the design is presented in Fig.4. The line at the gate of the FET is intended for the coupling of the NRC with the microstrip resonator.

The transistor connecting pads were taken into account in the modeling because of the wide frequency operating band of the transistor up to 20GHz.

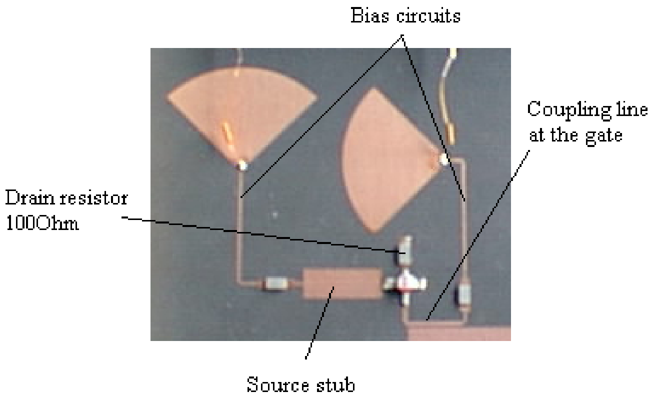

Fig.4. NRC topology

The following design steps are carried out to determine the parameters of the topology in Fig.4:

A. First Step

The S-parameters linear model of FHX35LG low noise FET is used. An on-chip 100 Ohm resistor is inserted at the drain of the FET to guaranty stability at this port. The resistor value is chosen in accordance with the drain transmission line (drain connector) impedance value. Simulation stability parameters K and B show that the resulting two-port (input = gate; output = source) is conditionally stable in the frequency range up to 8GHz (K<1). Consequently, stability must be guarantied in this frequency range with additional design steps.

B. Second Step

The schematic of Fig.3 is used to optimize the length of the stub at the source of the FET to have minimum noise measure of negative resistance at the gate at 3GHz. Initial $Re(Z_{11})$ and Rg values are chosen to 50 Ohm, and the start value of the transformer coefficient is one. The noise measure value reached is M=0.15. It is more than the M value of the FHX35LG itself (formulas in [6] gives a value of 0.11 for this device, however for ideal conditions).

C. Third Step

The nonlinear model of the FHX35LG FET available from Ansoft [9, pp.9-2] is used at this design step. The DC Nyquist Stability Analysis [9, pp.16-3 – 16-4] is used for the topology of Fig.4 to estimate the constraints on the length of the coupling line of the NRC. The Nyquist plots for various values of this length are presented in Fig.5. The circuit can be unstable if the Nyquist plot encircles the origin of the complex plane in a clockwise direction. So, cases a) and e) in Fig.5 are unstable cases and b), c) and d) correspond to stable cases. As a result, length of the coupling line of the NRC must be within the 6mm – 15.5mm range.

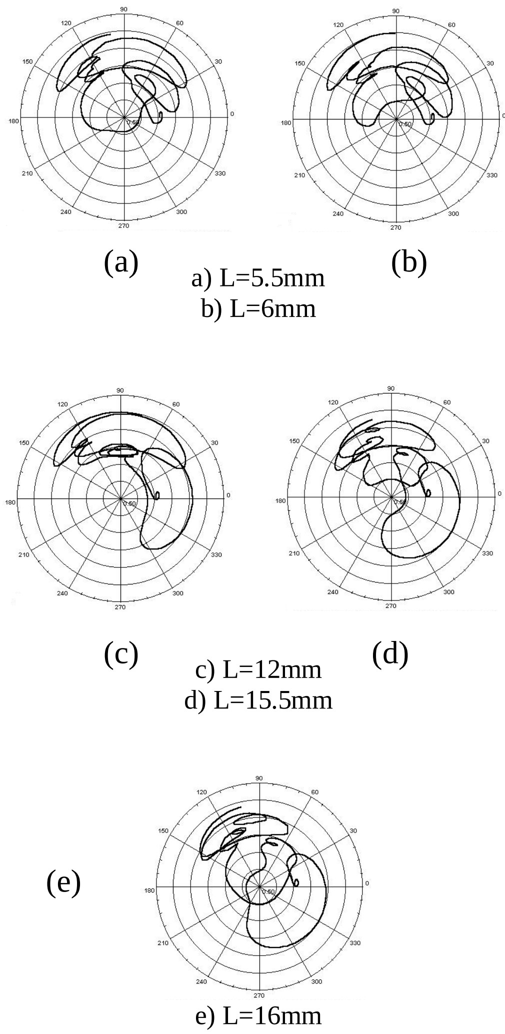

Fig.5. Nyquist plots for various values of the coupling line length L

Note that, bias circuits are taken into account in this analysis. This design step guaranties stability of NRC over the total FET operating frequency band. Then, the noise measure value of the NRC in the gate reference plane is M=0.15 at 3GHz. As mentioned above, with the condition M<<1, the impact of the NRC in the noise figure value of the MAF should be negligible as shown further.

IV. LOSS COMPENSATION OF A MICROSTRIP BANDPASS FILTER

A classical two resonator passive interdigitated filter [10] is chosen here as the passive part of the MAF designed. The NRC is coupled to the output resonator of the filter to compensate for losses of both passive resonators (Fig.4).

A photograph of the MAF is shown in Fig.6. The coupled lines parameters and resonators lengths have been optimized to obtain a 70MHz bandwidth at 3GHz. The length of the NRC coupling line has been optimized to compensate for the losses of the passive parts while taking into account the constraints obtained from DC Nyquist stability analysis.

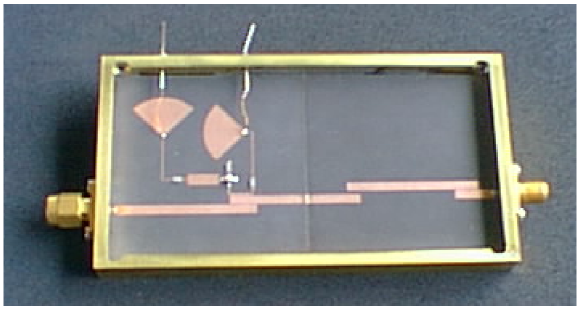

Fig.6. Topology of MAF with NRC coupled with the output resonator

The MAF has been fabricated on a Duroid substrate. Dimensions of the circuit are 2 inches by 4 inches. Post fabricate tuning of the resonators lengths has also been achieved to adjust the center frequency at 3 GHz, because of an inaccurate model of the coupling lines. Simulated and measured results are shown in Fig.7.

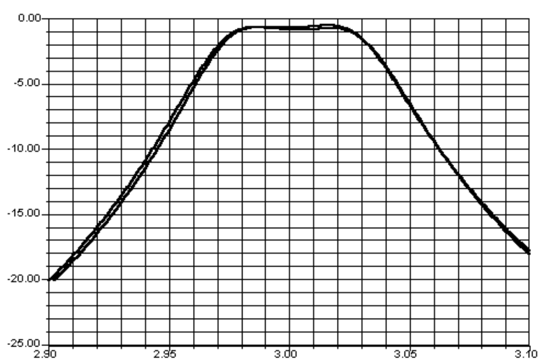

Fig.7. Simulation and measurement of S21 after tuning

An excellent agreement can be observed between simulated and experimental results after the tuning step. Measured insertion losses (-0.6dB) are due to the fact that circuit test fixture was not covered. Simulated and measured noise figures of the filter are reported in table 1. Table 1 also shows the noise figure of the MAF when the noise of the NRC is eliminated. Obviously, the contribution of the NRC in the noise figure of the MAF is negligible as expected. It can be seen in table 1, a good prediction of the MAF noise figure value in the passband with an accuracy of about 0.2dB. The impact of the NRC on the noise figure of the MAF is about 0.3dB.

Frequency (GHz)	Measured noise figure (dB)	Simulated noise figure (dB)	“passive“ noise figure (dB)
2.985	3.50	3.72	3.42
3.000	2.91	2.82	2.61
3.015	2.72	2.78	2.56

Table 1: Simulated and experimental noise figure of the MAF designed

V. CONCLUSION

We have presented a novel approach of low noise negative resistance circuit design. In thus approach, the design of a low noise NRC is critical when the NRC is designed for a MAF application. The NRC noise measure reduction has a direct impact on the MAF noise figure. This has been demonstrated and experimentally validated with the design of a hybrid low noise second-order filter using a single transistor at 3 GHz.

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